

ABOUT LDB

A compact data processing unit for Free Space Optical Communications and general purpose processing

The LDB is a powerful, compact and resilient programmable data processing unit for Free Space Optical communications (FSOC) and general purpose processing. Its primary purpose is to serve as a very low size, weight and power (SWaP) encoding and decoding capability for laser terminals, depoyable to ground, air, stratosphere and space. The hardware has been designed to support standards-compliant software to run on the AMD-Xilinx UltraScale+ on CPU and FPGA, which implements encoding and decoding processing for FSOC. Having been designed for Low Earth Orbit (LEO) missions, the LDB can be used with confidence at high and low altitudes, and in other harsh environments.

A Board Support Package is offered to support rapid development of third-party applications.

The LDB has the following technical features:

 Cubesat compatible form factor, adaptable to all platforms;

- Deploys standardised (i.e. SDA/CCSDS) or bespoke encoding and decoding processing software;
- Provides AMD-Xilinx UltraScale+ System on Chip for extensive data processing resources;
- Supports a wide set of data and signal interfaces including JTAG, Ethernet, UART and GPIO for debug, OBC Interface, I2C, CAN, UART, 4 GPIO;
- > High-speed serial interfaces for comms;
- Environmental resilience for space-to-space and space-to-ground satellite communications, or for communications between ground and airborne terminals and platforms.
- Remote Management and Fault Detection Isolation and Recovery (FDIR) including voltage, current and temperature reporting.







ALIGN MISSION CASE STUDY

Dual laser inter-satellite Free Space Optical Communications (FSOC)

The LDB will be utilised by the Northumbria University-led ALIGN mission. ALIGN will demonstrate a newly developed, FSOC device that uses an infrared laser source with innovative pointing techniques to transmit data up to 1 Gbps over 1000 km in LEO. The LDB will provide data processing for transmitting and receiving, as well as applying the required encoding and decoding to optical and data signals.



TECHNICAL SPECIFICATION

PROCESSING

- > System on Chip: Zynq UltraScale+ ZA5EV
- > RAM: 4GB LPDDR4 with ECC
- > Mass Memory: 2x 64GB eMMC with ECC
- > Boot Image Memory: 2x 256MB QSPI NAND
- > Boot Modes: JTAG, eMMC, QSPI NAND

PHYSICAL

- > Dimensions: 94 x 89 mm
- > Weight: Approx 300g

POWER

- > Input Voltage Supply: 5V
- > Redundant Input Supply: 12V
- > Max Power: 20W
- > Inrush and Ripple Limit: 200mA max on each supply
- > Current Draw Limit: 4A from 5V or 1.8A from 12V

INTERFACE

- > High Speed Serial: 4 Tx & Rx Pairs (up to 16.3 Gbps Each)
- > GPIO: 72 (FPGA HD Bank)
- Diagnostics: Dedicated diagnostics interfaces provides JTAG, Ethernet, UART and GPIO for debug. Interface designed to be

suitable for TVAC

 OBC Interface: 2x I2C, 2x CAN, UART, 4 GPIO (for controlling boot process)

BUILD OPTIONS

- Dual CAN bus options: CAN interfaces can be at assembly time configured to run as a redundant pair on a single bus or to operate on separate buses
- GPIO power level selection: GPIO lines can be at assembly line configured to run at 3.3V (max -70MHz) or 1.8V (max -250MHz)
- XilinX SoC grade selection: Automotive and commercial grades available
- Conformal coating: Boards available with and without coating selected for space usage

PROTOCOL STACK OPTIONS

 Can support both standardised (e.g. CCSDS O3K/SDA OCT) and bespoke encoder/decoder functionality including highthroughput Forward Error Correction (FEC)

HERITAGE AND STATUS

- Environmental Qualification: To be conducted Q1 2025 following ECSS guidance for LEO CubeSat missions
- Flight Heritage: Scheduled for usage within 2 UK space missions

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